AMENDMENTS

In the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application:

1. (Cancelled)

2. (Currently Amended) [[The]] A display device ~~of claim 1~~ comprising a plurality of pixels, each of the pixels comprising:

a serial-to-parallel converter converting a serial digital image signal supplied serially to the display device to a parallel digital image signal;

a DA converter converting the parallel digital image signal to an analog image signal; and

a pixel electrode configured to receive the analog image signal,

wherein the serial-to-parallel converter is connected to a drain signal line supplied with the serial digital image signal, and comprises a plurality of pixel selecting transistors connected to the drain signal line and a plurality of shift registers, each of the shift registers supplying a sampling pulse to a gate of [[the]] a corresponding pixel selecting transistor for sampling the serial digital image signal at a predetermined timing.

3. (Currently Amended) [[The]] A display device ~~of claim 1~~ comprising a plurality of pixels, each of the pixels comprising:

a serial-to-parallel converter converting a serial digital image signal supplied serially to the display device to a parallel digital image signal;

a DA converter converting the parallel digital image signal to an analog image signal; and

a pixel electrode configured to receive the analog image signal,

wherein the DA converter comprises a plurality of capacitor electrodes coupled with the pixel electrode, each of the capacitance electrodes having a weighted capacitance ratio to couple with the pixel electrode, and a clock supplying portion supplies a periodic clock signal to the capacitor electrodes in response to the parallel digital image signal.

4. (Previously Presented) The display device of claim 3, wherein areas of the capacitance electrodes are weighted to reflect corresponding bits of the parallel digital image signal.

5. (Currently Amended) A display device comprising:

a drain signal line configured to receive a serial digital image signal serially supplied to the display device;

a plurality of pixel selecting transistors connected to the drain signal line and selecting a pixel of the display device;

a plurality of shift registers, each of the shift registers supplying a sampling pulse to a gate of [[the]] a corresponding pixel selecting transistor for sampling the serial digital image signal at a predetermined timing to produce a parallel digital image signal;

a data retaining portion retaining the parallel digital image signal converted from the serial digital image signal;

a pixel electrode of the pixel;

a plurality of capacitor electrodes coupled with the pixel electrode, each of the capacitance electrodes having a weighted capacitance ratio to couple with the pixel electrode; and

a clock supplying portion supplying a periodic clock signal to the capacitor electrodes in response to the parallel digital image signal retained in the data retaining portion.

6. (Previously Presented) The display device of claim 5, wherein areas of the capacitance electrodes are weighted to reflect corresponding bits of the parallel digital image signal.

7. (Original) The display device of claim 5, wherein the data retaining portion comprises a capacitor.

8. (Original) The display device of claim 7, wherein the data retaining portion comprises at least one additional capacitor and the number of total capacitors in the pixel corresponds to the number of bits of the parallel digital image signal.

9. (Original) The display device of claim 5, wherein the data retaining portion comprises a static memory circuit.

10. (Original) The display device of claim 9, wherein the data retaining portion comprises at least one additional static memory circuit and the number of total static memory circuits in the pixel corresponds to the number of bits of the parallel digital image signal.